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2700
[2885/10] #6
278/111
12-13-98

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : VORBACH et al.
Serial No. : 08/947,254
Filed : October 8, 1997
For : I/O MEMORY BUS SYSTEM FOR DFPs AND UNITS
WITH TWO- OR MULTI-DIMENSIONAL
PROGRAMMABLE CELL ARCHITECTURES
Art Unit : 2818-2700

Assistant Commissioner
for Patents
Washington, D.C. 20231

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Date: 19 Nov 1998

Reg. No. 36,098

Signature:

[Signature]

Michelle M. Carniaux

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COMMUNICATION

S I R:

Applicant wishes to bring to the attention of the Examiner the following co-
pending applications:

U.S. Serial No. 08/544,435
U.S. Serial No. 08/946,810
U.S. Serial No. 08/947,002
U.S. Serial No. 09/000,724
U.S. Serial No. 08/946,998
U.S. Serial No. 08/946,999
U.S. Serial No. 09/145,139
U.S. Serial No. 08/946,812

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It is requested that each of these applications be considered and made of record herein.

Respectfully submitted,

KENYON & KENYON

By:

[Signature]
Michelle M. Carniaux (Reg. No. 36,098)

Dated: 19 Nov 1998

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